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The electrical performance of different channel thicknesses for IGZO thin film transistors

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Abstract

In this study, the I-V properties of bottom-gate InGaZnO (IGZO) thin-film transistors (TFTs) with different thicknesses of active-layer had been investigated. IGZO TFTs with variations in the IGZO layer thickness were deposited on bottom-gate-configuration SiN_X/glass substrates at 25 °C using radio frequency magnetron sputtering. We deposited the IGZO thicknesses with the range from 35 to 75 nm, and the ratio of gate width and gate length was 10. We found that the performance of devices was its thickness dependence. The best performance of IGZO TFT was found when the channel layer thickness was 50 nm, and it shows a threshold voltage of 5.18 V, a field-effect mobility in the saturation region of 0.21 cm^2/Vs, a subthreshold swing of 0.15 V/dec, and an I_{on}/I_{off} ratio is about 5.5×10^5.

Key words: InGaZnO, thin-film transistor, active-layer thickness

Introduction

Recently, the technology of transparent display has been developing rapidly. As a result, oxide semiconductors have come to be regarded as promising candidates for thin-film transistors (TFTs) because of their optical transparency in the visible range. Based on this fact, amorphous oxide thin-film transistors (OxTFTs) have been utilized in active-matrix liquid crystal displays (LCDs) and organic light-emitting diode displays (OLEDs), which combine the advantages of conventional amorphous Si (a-Si) TFTs and polycrystalline Si (p-Si) TFTs, while avoiding the drawbacks of both [1–5]. InGaZnO is the most attractive among the most of oxides materials because it shows high channel mobility, low subthreshold swing, and large area uniformity when used for channel layers. Because of the overlap of the spherical s-orbital of the heavy transition metal cations, a-IGZO possesses high mobility [6–8]. Several vacancies or interstitial defects influence the oxide films' electrical conductivity [9]. Generally, IGZO is sensitive to the film thickness and growth conditions. In this study, the radio frequency (RF) magnetron sputtering was used to deposit different thicknesses of IGZO film at room temperature and surveyed the correlation between the channel layer thickness and the electrical performance of the TFTs.

Experiments

The a-IGZO TFTs were fabricated on glass substrates. The device structure of the bottom-gate, top-contact, IGZO-based TFT is shown as a schematic in Fig 1. First, the glass substrates with a size of 2×2 cm^2 were cleaned using acetone, methanol, and de-ionized (DI) water sequentially in an ultrasonic bath to ensure the quality of the substrates. Then, the 70-nm-thick Al electrode was deposited using thermal evaporation as the bottom gate electrodes. The 200 nm SiN_x film as a gate dielectric layer was deposited by plasma enhanced chemical vapor deposition (PECVD) at a substrate temperature of 300 °C. The a-IGZO n-type channel layer with thicknesses of 35, 50, and 75 nm were deposited by RF sputtering with an IGZO (In_2O_3:Ga_2O_3:ZnO 1:1:1 mol%) target. This sputtering was performed at an RF power of 80 W, an Ar/O2 mixture gas ratio of 99/1 sccm, a working pressure of 5 mTorr, and a pre-deposition time of three minutes to remove the impurities of the target. Finally, we used the thermal evaporation to deposite 70-nm-thick Al as the source and drain (S/D) electrodes. We used an alpha-step to confirm the variations in IGZO film thickness. Both the a-IGZO channel and Al electrode contact areas were patterned through a shadow mask. The gate width (W) was 1 mm and gate length (L) was 100 μm.

The semiconductor parameter analyzer system (Agilent B1500A, Agilent Technologies) was used as a method to measure the electrical properties of a-IGZO TFTs a dark environment at atmospheric conditions.

Results and discussion

The I_{DS}-V_{DS} output curves of the IGZO TFTs with different thicknesses of channel layer from 35 to 75 nm are shown in Figs. 2(a)–(c). The drain current with a gate voltage 8V increased with the channel thickness up to 50 nm, and then decreased. According to our experimental results, the TFT with the 50 nm thickness for IGZO layer has the highest drain current 0.17 μA with an applied V_{GS} = 8 V at V_{DS}= 2V. The drain current level increased as V_{DS} increased up to 2V, and then it decreased. Since the TFT has the presence of the buried oxide, the heat generated by the element during operation was not easily dissipated, and it accumulated in the element. As a result, its temperature rose, and a self-heating phenomenon occurred. In another study [10], the SHE(Self-Heating Effect) was compared with respect to different growth temperatures of the device. The creation of more free carrier and grain boundaries in the channel layer induced the heating effect as the growth temperature of the semiconductor layer too low. These defects can form a trap, extend the resistance, and raise the temperature along the channel path to generate further defects, which in turn decrease the charge density, thus

reducing the mobility of the channel layer [10].

The corresponding transfer characteristics of I_{DS}-V_{GS} curves with V_{DS} = 8 V and the $I_{DS}^{1/2}$-V_{GS} curves of the TFTs with different channel thicknesses are shown in Figs. 3(a) and (b). The I_{on}/I_{off} ratio for 35 nm, 50 nm, and 75 nm IGZO TFT is measured to be about 3.4×10^4, 5.5×10^5, and 3.4×10^4, respectively. As the channel layer thickness increased from 35 to 75 nm, the off current (I_{off}) of TFTs increased from 1.14×10^{-12} to 6.18×10^{-12}A. Fig. 3(b) showed the $I_{DS}^{1/2}$-V_{GS} curves, we defined the threshold voltage (V_{TH}) by the following method. First, we plotted the tangent line of the $I_{DS}^{1/2}$-V_{GS} curves, and then we defined the intersection of the tangent line and the V_{GS}-axis as the threshold voltage (V_{TH}). As for the field effect mobility (μ) in saturation region, it can be cited according to the following formula:

$$\mu_{FE} = \frac{Lg_m}{WC_{ox}(V_{GS}-V_T)} \quad (V_{DS}>V_{GS}-V_{TH}) \tag{1}$$

where C_{ox} is the capacitance per unit area of the gate insulator (C_{ox} = 0.31mF/m^2). W/L is the device aspect ratio with W =1 mm and L = 100 μm, V_{DS} is the voltage of drain to source, and V_{GS} is the voltage of gate to source. Another important parameter to look at in evaluating the quality of device is the subthreshold swing (SS). We can obtain the value from the inverse of maximum slope of the transfer curve in semi-log I_{DS}-V_{GS} by following equation [11]

$$SS = \frac{dV_{GS}}{d(LogI_{DS})} \tag{2}$$

SS represents how rapidly I_{DS} increases by one order with V_{GS}. The electrical performances of various channel thicknesses are listed in Table I.

Figs. 4(a) and (b) show the variations of electrical properties owing to the change of channel thickness. As shown in Fig. 4(a), the V_{TH} decreases as the active layer thickness increases up to 50 nm. However, V_{TH} increases as the thickness increases further from 50 nm. Generally, when the channel layer thickness increases, the number of free carriers might increase as well, which would cause the decrease of V_{TH}. Besides, with the increase in channel thickness to 75 nm, it was brought on the rise in V_{TH}. It may be caused by the semi-insulating characteristics of the IGZO channel layer [11].

As for the field effect mobility, we found that the mobility increases as IGZO thickness increases until 50 nm and then decreases. Usually, lower carrier mobility is found in thinner IGZO films. This is caused by the fact that when the carrier transport layer is further away from the thicker film surface, the effect of surface roughness on carrier mobility is weaker in thicker films than in thinner films [12,13]. However, we speculated that self-heating phenomenon was responsible for the decrease in the field effect mobility in the channel thickness at 75 nm. The SHE brought about the defects which in turn decreased the charge density, and thus the mobility of the channel layer.

From the results of Fig. 4(b), we can observe that the I_{on}/I_{off} ratio increases as the thickness of the active layer increases. Nonetheless, the degradation of the TFT performance is caused by the increase in channel thickness because of the increase in the I_{off} , which shows that the active layer should be as thin as possible in order to reduce the power consumption. Simultaneously, the higher I_{off} might cause a deterioration in the subthreshold swing. For films thinner than 50 nm, the SS does not change significantly. As the channel thickness increases from 50 to 75 nm, the SS increases insignificantly, from 0.15 to 0.64 V/dec. The value of subthreshold swing is a sign of the total trap state density (N_t) and the interface states at or near the interface between IGZO and SiN_x are included. The SS is related to N_t as expressed by the following equation:

$$SS = \frac{KT}{qlog(e)}\left[1+\frac{q}{C_{ox}}N_t\right] \tag{3}$$

where C_{ox} is the capacitance per unit area of the dielectric layer, K is the Boltzmann constant, and q is the elementary charge, and T is the temperature. We found that the thicker film devices exhibited a deterioration in the subthreshold swing as the film increased in thickness. This contributed to a combination of effects: I_{off} increased and total trap state density N_t increased as well . The explicit mechanism by which the large I_{off} brought about the degeneration of SS can be obtained from.

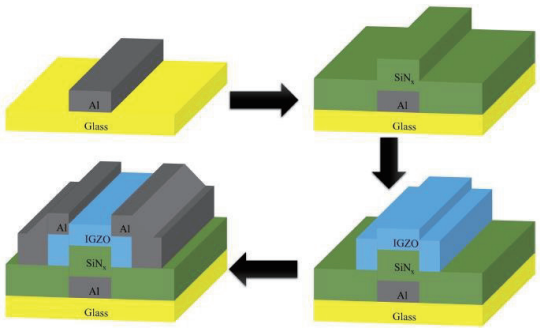
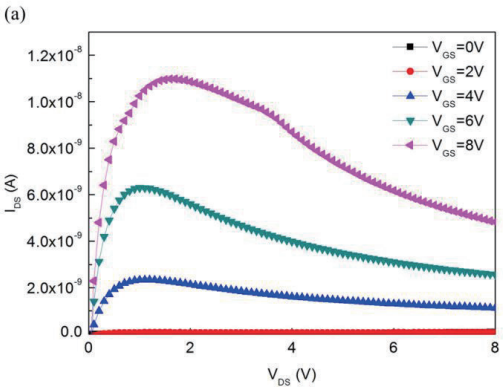


Fig. 1. The fabrication process of the InGaZnO TFT devices that shown by schematic diagram



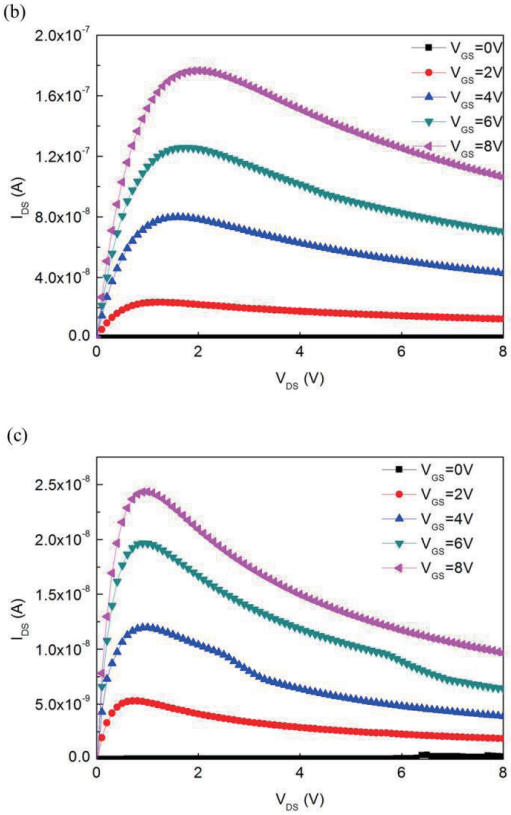
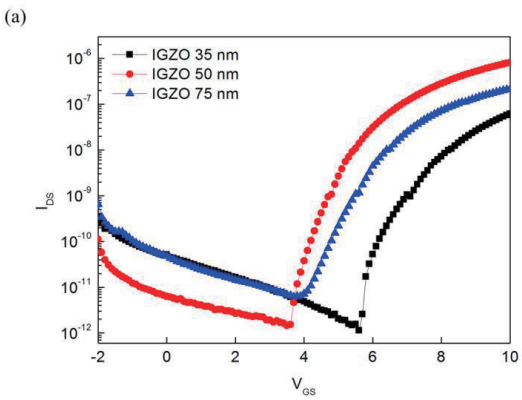


Fig. 2. I_{DS}–V_{DS} transfer characteristics of different IGZO channel thicknesses (a) 35, (b) 50, and (c) 75 nm



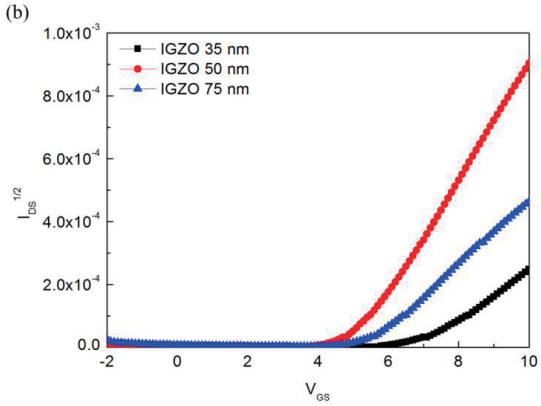
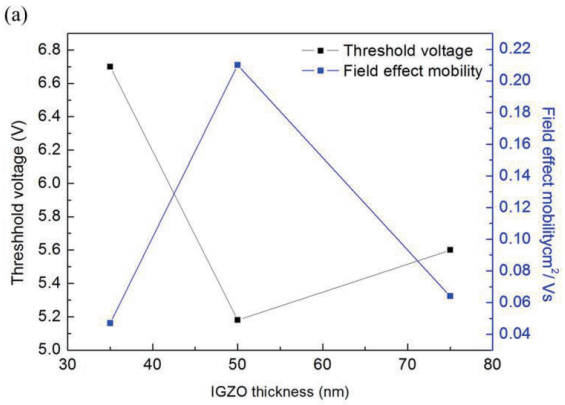


Fig. 3. Transfer characteristics of different IGZO thicknesses at V_D = 8 V (a) I_{DS}-V_{GS} (b) $I_{DS}^{1/2}$-V_{GS}



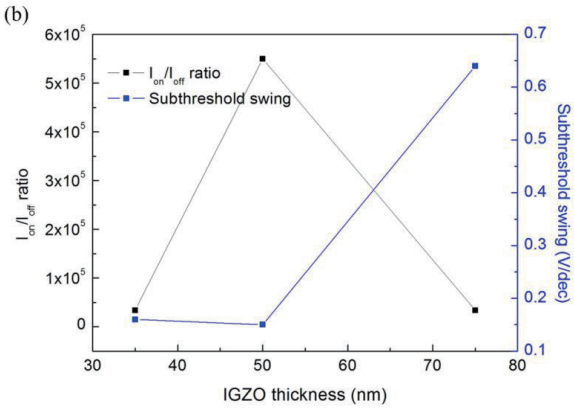


Fig. 4. The electrical parameters of different IGZO channel thicknesses (a) field effect mobility and threshold voltage and (b) subthreshold swing and I_{on}/I_{off} ratio.

TABLE I. The electrical performance of various channel thickness

IGZO thickness (nm)	V_{th} (V)	Mobility ($cm^2/V\ s$)	Nt cm^{-2}	On/off ratio	SS (V/decade)	I_{on} (A)	I_{off} (A)
35	6.7	0.047	1.14×10^{12}	3.4×10^{4}	0.16	6.16×10^{-8}	1.14×10^{-12}
50	5.18	0.21	2.7×10^{11}	5.5×10^{5}	0.15	8.15×10^{-7}	1.46×10^{-12}
75	5.6	0.06	1.14×10^{12}	3.4×10^{4}	0.64	2.16×10^{-7}	6.18×10^{-12}

. Conclusion

We examined the electrical properties of the IGZO TFTs with various active layer thicknesses. The threshold voltage, mobility, on/off drain current, and subthreshold swing can be modified by varying the thickness of the IGZO film. The optimal channel thickness was 50 nm, which showed a field-effect mobility in the saturation region of 0.2 cm^2/Vs, a threshold voltage of 5.18 V, a drain current I_{on}/I_{off} ratio of approximately 5.5×10^5, and a subthreshold swing of 0.15 V/dec. Our device showed relatively low field-effect mobility, which was due to that we did not do the annealing process after the device complicated, and this might lead to the significant self-heating effect.

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