ISBN: 978-981-14-2136-5

The Degradation Induced by Hot-Carrier Injection in 130-nm Partially Depleted SOI pMOSFETs Fabricated on Modified Wafer

Huilong Zhu[1, 2, a, *], Dawei Bi[1, b, *], Zhiyuan Hu[1, c], Xin Xie[1, 2, d], Zhengxuan Zhang[1, e], Shichang Zou[1, f]

[1]State Key Laboratory of Functional Materials for Informatics, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai 20050，China
[2]University of Chinese Academy of Sciences, Beijing 10004, China
[a]zhuhuilong@mail.sim.ac.cn, [b]davidb@mail.sim.ac.cn, [c]zyhu@mail.sim.ac.cn,
[d] xiexin@mail.sim.ac.cn, [e]zxzhang@mail.sim.ac.cn, [f]zsc@mail.sim.ac.cn

Abstract

The hot carrier effect of 130-nm partially depleted SOI pMOSFETs fabricated on wafer modified by silicon ions implantation is reported in this paper. Due to the electron traps in the buried oxide, the degradation induced by hot-carrier injection is anomalous. Specifically, at low V_g stress, the positive degradation of modified pMOSFETs is faster and more serious than control devices, and huge leakage current is found after a period of stress time. Moreover, at a $V_g = V_d$ stress, the control pMOSFETs present lightly negative degradation, while the modified pMOSFETs present enormous positive degradation. Finally, a reasonable interpretation is proposed that the deep electron traps in the buried oxide can capture hot electrons during the stress, which will cause the back channel exhausted even inversed and enhance the coupling effect between the front gate and the back gate.

Key words: Hot-carrier effects, PD-SOI, pMOSFETs, silicon ions implantation.

Introduction

SILICON-on-Insulated (SOI) device has important applications in radiation-hardened military and space field due to its inherent advantages of small capacitance, superior subthreshold characteristics, eliminating the latch-up effects, excellent resistances to irradiation, etc. [1]. However, since the thick buried oxide layer (BOX) could trap positive charges included by radiation, the SOI devices are more sensitive to total dose radiation environments than bulk-silicon devices [2]. Fortunately, implanting silicon ions into the BOX is a proved method, reported by many paper, which can form silicon nanometer clusters in the box as deep electron traps to capture electrons to compensate the trapped positive charges during irradiation [3], [4]. Nevertheless, few literatures have detailed the threat to device reliability caused by these deep electron traps. In this paper, we focus on the degradation induced by hot-carrier injection in 130-nm partially depleted SOI pMOSFETs fabricated on wafer modified by silicon ions implantation and reveal its different degradation compare with normal devices.

Experimental details

The control wafer used in our experiment is 200-mm diameter UNIBOND® wafer from SOITEC Corporation with 100-nm top silicon and 145-nm BOX thickness. And the modified wafer is fabricated by implant silicon ions into the BOX. All the devices are fabricated on the 130 nm partially depleted SOI technology with typical shallow trench isolation. T-shape gate is used for body contact. The thickness of gate oxide is about 6.4 nm and the operating voltage is 3.3V. The length of the devices is 10 μm, and the width is 0.3 μm. All the experiments were performed on wafer level with back gate grounded. I_d-V_g curve and saturation drain current (I_{ds}) were measured after a stress time of 10s, 30s, 50s, 100s, 300s, 1000s and 3000s. Then, V_t and $G_{m,\,max}$ were determined according to the I_d-V_g curves. For eliminating the impact of the measurement process, the gate voltage was just sweep to -1.5V while drain voltage was fixed at -0.1V to get I_d-V_g curve, and one-point test process was applied to get I_{ds}, i.e., I_{ds} was directly measured after high voltages being applied to the gate and drain, rather than sweeping drain voltage to -3.3V while gate was fixed at -3.3V.

Result and discuss

A. Low V_g stress

Firstly, low V_g stress (V_g = -0.62 V, V_d = -4.8 V) was imposed on the pMOSFETs until 3000s.

Fig.1 shows the I_d-V_g (V_d = -0.1 V) characteristics of these pMOSFETs fabricated on control and modified wafer after different stress time. For control devices, the I_d-V_g curves have a lightly positive shift after stress. However, for modified devices, apart from more enormous positive shift, huge leakage current is observed after a period of stress time. The stress time dependence of the shift of V_t, I_{ds}, and $G_{m,\,max}$ is shown in Fig.2. As a matter of convenience, we define a positive degradation as $|V_t|$ decreasing, I_{ds}, and $G_{m,\,max}$ increasing. On the contrary, the negative degradation is defined as $|V_t|$ increasing, I_{ds} and $G_{m,\,max}$ decreasing. As shown in Fig.2, the positive degradations of V_t and I_{ds} of modified devices are nearly two times greater than those of control devices, which confirms the different shifts of I_d-V_g curves in Fig.1. However, the shifts of $G_{m,\,max}$ are comparable between these two kinds of devices, indicating that the degradations of the gate oxide between them are at the same level.

This can be simply explained as the following. At low stress V_g, for control devices, the hot electrons induced by impact

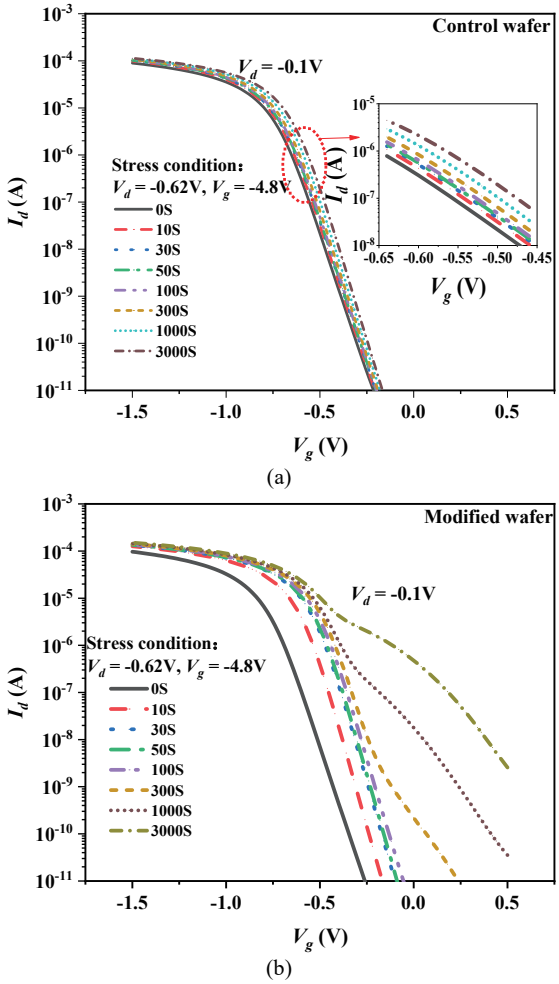

Fig.1 I_d-V_g (V_d = -0.1 V) curves of the pMOSFETs fabricated on control (a) and modified (b) wafer after a stress time of 10s, 30s, 50s, 100s, 300s, 1000s and 3000s (stress condition: V_g = -0.62 V, V_d = -4.8 V).

ionization and interface traps are the dominant mechanism of the device degradations. These hot electrons, trapped at the-interface near the drain, leads to a decrease of the effective channel and positive degradation. Nevertheless, the interface traps can reduce the mobility of the channel carrier. Finally, a positive degradation emerges because the latter's influence is masked by the former [5], [6]. On the other hand, the electron injection can also happen at the Top-Si/BOX interface. However, due to the high quality of the interface of UNIBOND SOI wafer, its influence to the front channel of partially depleted SOI devices is small [6], [7].As for modified devices, the degradation of the gate oxide is similar to the control devices, while the degradation of the back channel is of great different. According to the previous papers, Silicon ions implantation can form silicon nanometer clusters in the box as deep electron traps. While, at the meantime, the implantation also induces amount of shallow electron traps near the Top-Si/BOX interface [8]. It can be speculated that this abnormal degradation and huge leakage current is induced by those electron traps. Firstly, when the voltage of the drain terminal is stressed at a high level (V_d = -4.8 V in this paper), amount of hot electrons are created by impact ionization due to the strong electric field strength along the channel. And the generated electrons are swept away by the drain terminal. Next, these hot electrons induced by impact ionization can be easily captured by the shallow electron traps near the Top-Si/BOX interface. Moreover, the electron traps in the BOX can also capture electrons tuning into the BOX under the vertical electric field. These captured electrons cause the back channel exhausted and enhance the coupling effect between the front and back gate, which leading to the enormous positive degradation. And, when the devices are stressed long enough, these trapped electrons even cause the back channel inversed. Thus, the devices become unable to shut off.

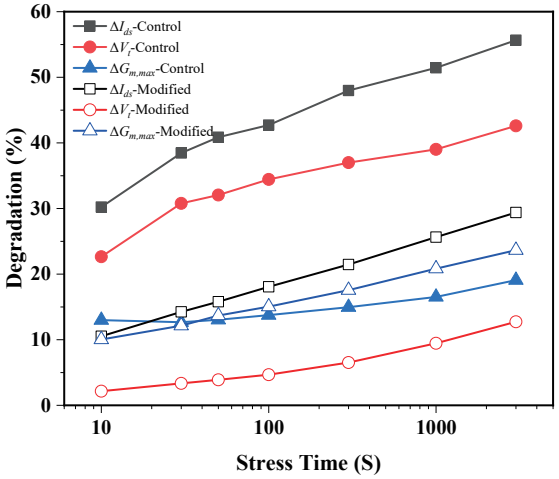

Fig.2 Stress time dependence of V_t, I_{ds}, and $G_{m,\,max}$ degradation for control and modified devices (stress: V_g = -0.62 V, V_d = -4.8 V).

B. High V_g stress

Else, high V_g stress (V_g = V_d = -4.8 V) is also imposed on these different devices.

The I_d-V_g (V_d = -0.1 V) curves of them are shown in Fig.3. The control devices have extremely tiny negative shift. But the modified devices still show obvious positive shift. And the stress time dependence of the shifts of V_t, I_{ds}, and $G_{m,\,max}$ are shown in Fig.4. For control devices, the negative shifts of V_t, and I_{ds} are too lightly to distinguished. Luckily, the $G_{m,\,max}$ shows a largish reduction. However, the modified devices still present a huge increasing of V_t, and I_{ds}, while the $G_{m,\,max}$ appears a reduction after the initial increasing.

At high stress V_g, for the control devices, there is no longer any electron trapping happened, and the interface traps plays an important role of the negative shift by reducing the mobility of the carriers [9]. For modified devices, on the one hand, there are still number of hot electrons induced by impact ionization being trapped by the electron traps near the Top-Si/BOX interface. And this trapped electrons cause the positive degradation of the V_t and I_{ds}. However, for the $G_{m,\,max}$, the initial increasing is a result of the severe reduction of the V_t, and the

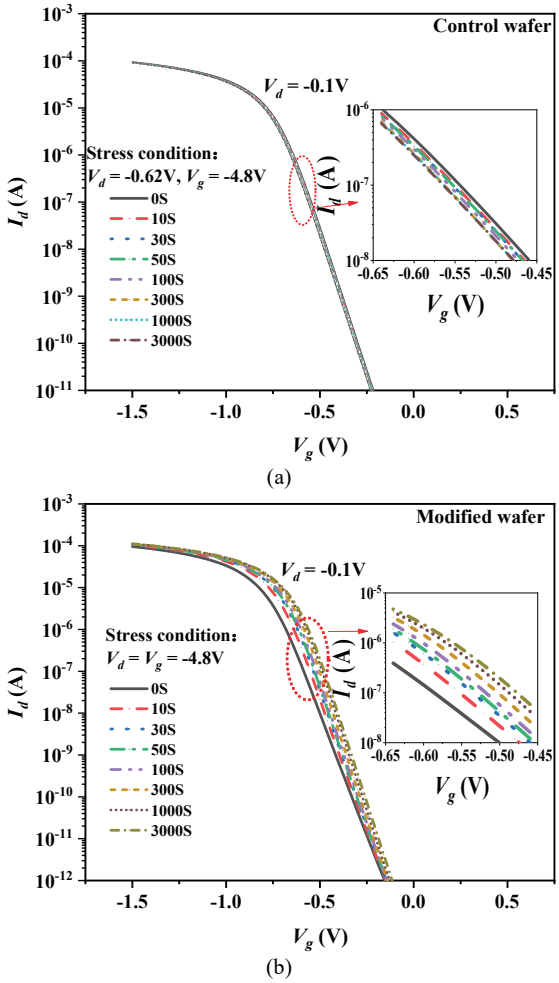

Fig.3 I_d-V_g (V_d = -0.1 V) curves of the pMOSFETs fabricated on control (a) and modified (b) wafer after a stress time of 10s, 30s, 50s, 100s, 300s, 1000s and 3000s (stress condition: V_g = V_d = -4.8 V).

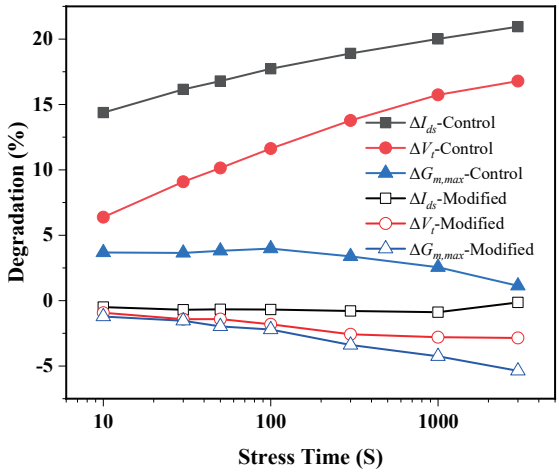

Fig.4 Stress time dependence of V_t, I_{ds}, and $G_{m,\,max}$ degradation for control and modified devices (stress: V_g = V_d = -4.8 V).

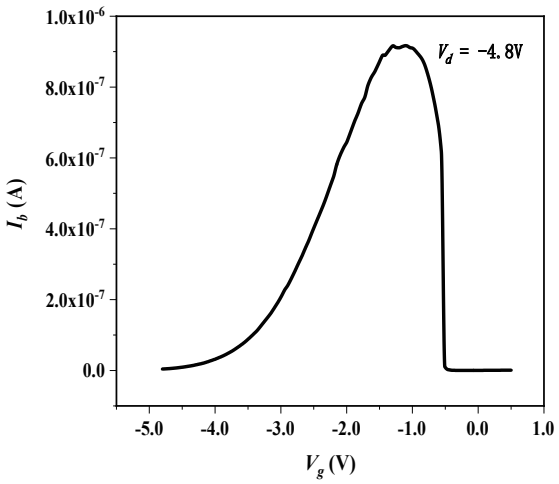

Fig.5 I_b-V_g (V_d = -4.8V) curves of the modified devices. The I_b at V_g= -0.62V is an order of that at V_g= -4.8V.

subsequent decreasing reveals the degradation of the carriers' mobility same as the control devices. On the Others hand, as shown in Fig.5, the substrate current under high stress V_g (V_g = V_d = -4.8 V) is several order of magnitude smaller than that under low stress V_g (V_g = -0.62V, V_d = -4.8 V), which means that the quantity of the trapped electrons in the BOX under such high stress V_g is also several order of magnitude smaller than that under low stress. Therefore, the trapped electrons are not enough to cause the back channel inversed. That's why no obvious increasing of leakage current is found after a long stress time.

Conclusion

The degradation induced by hot-carrier injection in 130-nm PD SOI pMOSFETs fabricated on wafer modified by silicon ions implantation has been present in this paper. Silicon ions implantation will induce amount of shallow electron traps near the Top-Si/BOX interface and deep electron traps in the BOX. And these electron traps, especially the former, can easily capture hot electrons induced by impact ionization. At low stress V_g, the numerous trapped electrons make the back channel exhausted even inversed and enhance the coupling effect between the front and back gate, which induces a faster and more serious positive degradation and huge leakage current. And at high stress V_g, due to the fact that the quantity of the trapped electrons in the BOX is several order of magnitude smaller, the trapped electrons are not enough to cause the back channel inversed. Thus, only enormous positive degradation is still observed while without an obvious increasing of the leakage current.

References

[1] Schwank, J. R., V. Ferlet-Cavrois, M. R. Shaneyfelt, P. Paillet, and P. E. Dodd. "Radiation effects in SOI technologies." *IEEE*

Transactions on Nuclear Science 50, no. 3 (2003): 522-538.

[2] Barnaby, H. J. "Total-Ionizing-Dose Effects in Modern CMOS Technologies." *IEEE Transactions on Nuclear Science* 53.6(2006):3103-3121.

[3] Mrstik, B. J, et al. "Electron and hole trapping in thermal oxides that have been ion implanted." *Microelectronic Engineering* 59.1–4(2001):285-289...

[4] Mrstik, B. J., H. L. Hughes, P. Gouker, R. K. Lawrence, and P. J. McMarr. "The role of nanoclusters in reducing hole trapping in ion implanted oxides." *IEEE Transactions on Nuclear Science* 50, no. 6 (2003): 1947-1953.

[5] Renn, Shing-Hwa, Christine Raynaud, J-L. Pelloie, and Francis Balestra. "A thorough investigation of the degradation induced by hot-carrier injection in deep submicron N-and P-channel partially and fully depleted unibond and SIMOX MOSFETs." *IEEE Transactions on Electron Devices* 45, no. 10 (1998): 2146-2152.

[6] Koyanagi, Mitsumasa, Alan G. Lewis, Russel A. Martin, Tiao-Yuan Huang, and John Y. Chen. "Hot-electron-induced punchthrough (HEIP) effect in submicrometer PMOSFET's." *IEEE Transactions on Electron Devices* 34, no. 4 (1987): 839-844.

[7] Nazarov, Alexei N., Yuri Houk, and Valeriya I. Kilchytska. "High-field current transport and charge trapping in buried oxide of SOI materials under high-field electron injection." *Journal of Telecommunications and Information Technology*(2004): 50-61.

[8] Huang, Huixiang, Dawei Bi, Ming Chen, Yanwei Zhang, Xing Wei, Zhiyuan Hu, and Zhengxuan Zhang. "Improving total dose tolerance of buried oxides in SOI wafers by multiple-step Si+ implantation." *IEEE Trans. Nucl. Sci* 61, no. 3 (2014): 1400-1406.

[9] Heremans, Paul, Rudi Bellens, Guido Groeseneken, and Herman E. Maes. "Consistent model for the hot-carrier degradation in n-channel and p-channel MOSFETs." *IEEE Transactions on Electron Devices* 35, no. 12 (1988): 2194-2209.